

What is claimed is:

1. An NROM transistor comprising:  
an ultra-thin silicon-on-insulator layer having two source/drain regions separated  
by a normally fully depleted body region;  
an oxide layer formed above each of the source/drain regions;  
a gate insulator formed over the body region and oxide layer, the gate insulator  
capable of storing a plurality of charges; and  
a control gate formed on the gate insulator.
2. The transistor of claim 1 wherein the gate insulator is an oxide-nitride-oxide  
composite structure.
3. The transistor of claim 1 wherein the gate insulator layer is a composite layer  
comprised of one of an oxide-nitride-aluminum oxide composite layer, an oxide-  
aluminum oxide-oxide composite layer, or an oxide-silicon oxycarbide-oxide  
composite layer.
4. The transistor of claim 1 wherein the gate insulator layer is a non-composite layer  
comprised of one of silicon oxides formed by wet oxidation and not annealed,  
silicon-rich oxides with inclusions of nanoparticles of silicon, silicon oxynitride  
layers, silicon-rich aluminum oxide insulators, silicon oxycarbide insulators, or  
silicon oxide insulators with inclusions of nanoparticles of silicon carbide.
5. The transistor of claim 1 wherein the gate insulator is comprised of non-  
stoichiometric single layers of two or more of silicon, nitrogen, aluminum,  
titanium, tantalum, hafnium, lanthanum, or zirconium.
6. The transistor of claim 1 wherein the transistor has a planar structure.

7. The transistor of claim 1 wherein the transistor has a NAND architecture.
8. The transistor of claim 1 wherein the transistor has a NOR architecture.
9. An NROM flash memory cell comprising:
  - a substrate comprising an insulator layer and a silicon-on-insulator layer that has a thickness less than 100 nm, the silicon-on-insulator layer comprising two source/drain regions separated by a normally fully depleted body region;
  - an oxide layer formed above each of the source/drain regions;
  - a composite gate insulator formed over the body region and oxide layer, the gate insulator having a nitride layer capable of storing a first charge when the cell is operated in a first direction and a second charge when the cell is operated in a second direction; and
  - a control gate formed on the composite gate insulator.
10. The cell of claim 9 wherein the control gate is comprised of a polysilicon material.
11. The cell of claim 9 wherein a first source/drain regions operates as a drain region when the cell is operated in the first direction and as a source region when the cell is operated in the second direction.
12. A vertical NROM flash memory array comprising
  - a substrate having a first plurality of source/drain regions;
  - an oxide pillar extending outward from the substrate;
  - a plurality of ultra-thin silicon body regions, each comprising epitaxial regrowth of silicon along opposite sidewalls of the oxide pillar, each body region extending vertically from a different source/drain region;
  - a second plurality of source/drain regions formed on the oxide pillar, each source/drain region coupled to a different body region;

an insulator layer formed over the first plurality of source/drain regions, the plurality of body regions, and the second plurality of source/drain regions; and  
a control gate formed over the insulator layer.

13. The array of claim 12 wherein a first transistor of the memory array is comprised of a first source/drain region from the first plurality of source/drain regions, a first ultra-thin silicon body region, a first source/drain region from the second plurality of source/drain regions, a portion of the insulator layer over the first silicon body region, and a portion of the control gate over the portion of the insulator layer.
14. The array of claim 12 wherein the insulator layer is comprised of a composite oxide-nitride-oxide structure.
15. The array of claim 14 wherein the lower oxide layer has a greater thickness in a trench on either side of the oxide pillar than a remaining portion formed around the oxide pillar.
16. The array of claim 15 wherein the first plurality of source/drain regions is isolated between each trench.
17. A vertical NROM flash memory array comprising  
a substrate having a lower source/drain region;  
an oxide pillar extending outward from the substrate above the lower source/drain region;  
a plurality of ultra-thin silicon body regions, each comprising epitaxial regrowth of silicon along opposite sidewalls of the oxide pillar, each body region extending vertically from each side of the lower source/drain region;  
an upper source/drain region formed on the oxide pillar, each side of the upper source/drain region coupled to a different body region;

an insulator layer formed around either side of the lower source/drain region, the plurality of body regions, and the upper source/drain region, portions of the insulator layer on each side of the lower source/drain region having a greater thickness than the remaining insulator layer such that the lower source/drain region is isolated between the thicker insulator layer portions; and  
a control gate formed over the insulator layer.

18. The memory array of claim 17 wherein the thicker insulator layer portions are a lower oxide layer.
19. A vertical NROM flash memory array comprising:
  - a substrate having a doped region of a different conductivity type than the substrate extending along the substrate, the doped region acting as a first source/drain region;
  - a plurality of oxide pillars extending from the first source/drain region;
  - a plurality of ultra-thin silicon body regions each formed along an opposing sidewall of an oxide pillar, each ultra-thin silicon body region being fully depleted;
  - a polysilicon material formed on top of each oxide pillar and each body region, the polysilicon material acting as a second source/drain region and having the same conductivity type as the first source/drain region;
  - an oxide layer formed over the substrate, body regions, and second source/drain regions such that the oxide layer has a greater thickness along the substrate than in other areas;
  - a nitride-oxide layer formed over the oxide layer only on the opposing sides of the oxide pillar; and
  - a polysilicon control gate formed over the nitride-oxide layer.

20. The memory array of claim 19 and further including a conductive wire coupling the second source/drain regions on each oxide pillar.
21. The memory array of claim 19 wherein the first and second source/drain regions are n+ type conductive material.
22. The memory array of claim 19 wherein the array has a NOR type architecture.
23. An electronic system comprising:  
a processor that generates control signals for the system; and  
a memory array coupled to the processor and having a plurality of memory cells comprising:  
an ultra-thin silicon-on-insulator layer having two source/drain regions separated by a normally fully depleted body region;  
an oxide layer formed above each of the source/drain regions;  
a gate insulator formed over the body region and oxide layer, the gate insulator capable of storing a plurality of charges; and  
a control gate formed on the gate insulator.
24. A method for forming an array of NROM flash memory cells, the method comprising:  
forming a plurality of doped regions in an ultra-thin silicon-on-insulator, the silicon-on-insulator having a fully depleted body region;  
forming an oxide layer above each of the plurality of doped regions;  
forming a gate insulator layer over the doped regions and the fully depleted body region; and  
forming a polysilicon control gate over the gate insulator layer.
25. The method of claim 24 wherein forming the gate insulator comprises forming an oxide-nitride-oxide layer.

26. The method of claim 24 wherein the polysilicon control gate is formed such that the array is a NOR flash memory array.
27. The method of claim 24 wherein the polysilicon control gate is formed such that the array is a NAND flash memory array.
28. A method for forming a memory array comprising a plurality of vertical NROM memory cells, the method comprising:  
forming a first plurality of doped regions in a substrate such that a gap exists between each doped region, the doped regions having a different conductivity type than the substrate;  
forming an oxide pillar over the gap between the doped regions;  
forming an ultra-thin silicon body region by epitaxial regrowth extending from each doped region along opposing sidewalls of the oxide pillar;  
forming a second plurality of doped regions in a polysilicon material over the oxide pillar and body regions such that the doped regions over the pillar are electrically coupled and have the same conductivity type as the first plurality of doped regions;  
forming a gate insulator layer over the first plurality of doped regions, the body regions, and the second plurality of doped regions; and  
forming a polysilicon control gate area over the gate insulator adjacent to each of the body regions.
29. The method of claim 28 wherein the forming of the polysilicon control gate area includes forming the control gate as a continuous layer over the gate insulator.
30. A method for forming a memory array comprising a plurality of vertical NROM memory cells, the method comprising:

forming a first plurality of doped regions in a substrate, the doped regions having a different conductivity type than the substrate;

forming an oxide pillar over each doped region such that each end of each doped region extends beyond an adjacent sidewall of the oxide pillar;

forming an ultra-thin silicon body region by epitaxial regrowth extending from the ends of the doped regions and along opposing sidewalls of the oxide pillar;

forming a second plurality of doped regions in a polysilicon material over the oxide pillar and body regions such that the doped regions over the pillar are electrically coupled and have the same conductivity type as the first plurality of doped regions;

forming a gate insulator layer over the first plurality of doped regions, the body regions, and the second plurality of doped regions, the gate insulator layer having a lower layer, adjacent to each end of a doped region of the first plurality of doped regions, that has a thickness greater than remaining portions of the lower layer; and

forming a polysilicon control gate area over the gate insulator adjacent to each of the body regions.

31. The method of claim 30 wherein the gate insulator layer is a composite oxide-nitride-oxide layer and the lower layer is the oxide layer.
32. The method of claim 30 wherein the lower layer is an oxide layer.